




Helping Customers Innovate, Improve & Grow



### Description

Vectron's VC-708 Crystal Oscillator is a quartz stabilized, low phase noise, differential output oscillator which is hermetically sealed in a 5x7 ceramic package.

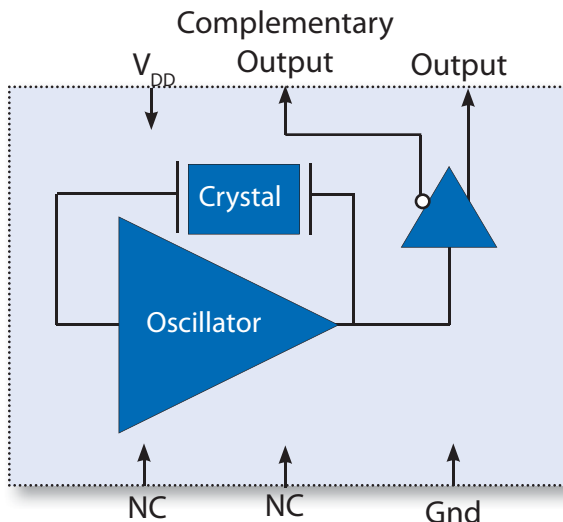
### Features

- 47 fs RMS jitter typical, 12kHz-20MHz
- Ultra Low Jitter Performance, 3rd OT Crystal Design
- Differential Output
- Low Current Consumption
- -10/70°C or -40/85°C Operation
- Hermetically Sealed 5x7 Ceramic Package
- Product is compliant to RoHS directive  and fully compatible with lead free assembly

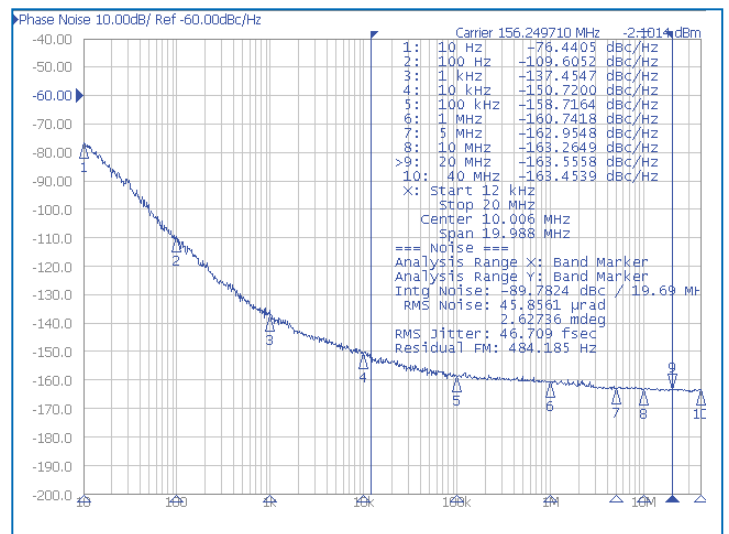
### Applications

- Ethernet, GbE, SynchronE
- Fiber Channel
- PON
- Driving A/D's, D/A's, FPGA's
- Test and Measurement
- Medical
- Storage Area Networking
- Telecom
- COTS

### Block Diagram



### Phase Noise Plot

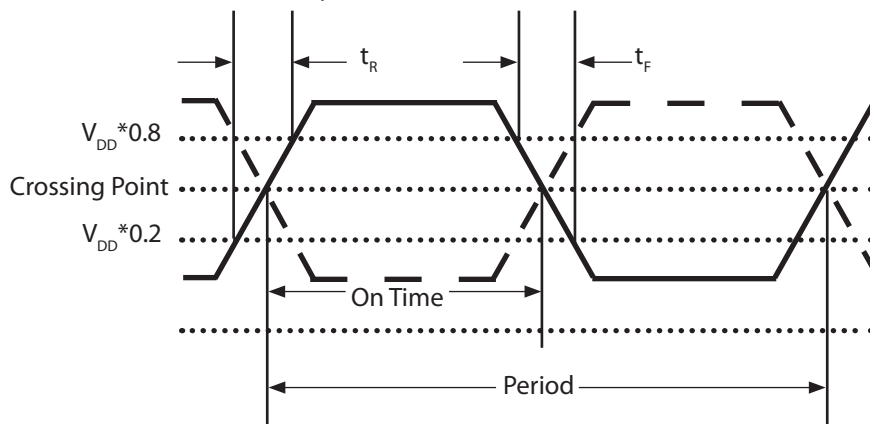


# Performance Specifications

**Table 1. Electrical Performance, LVPECL**

Parameter	Symbol	Min	Typical	Maximum	Units
<b>Supply</b>					
Voltage <sup>1</sup>	$V_{DD}$	3.135 2.375	3.3 2.5	3.465 2.625	V V
Current (No Load)	$I_{DD}$		50	65	mA
<b>Frequency</b>					
Nominal Frequency	$f_N$	See Table 8.			MHz
Stability <sup>2</sup> (Ordering Option)		±25, ±50, ±100			ppm
<b>Outputs</b>					
Output Logic Levels, -10/70°C					
Output Logic High	$V_{OH}$	$V_{DD}-1.025$		$V_{DD}-0.880$	V
Output Logic Low	$V_{OL}$	$V_{DD}-1.810$		$V_{DD}-1.620$	V
Output Logic Levels, -40/85°C					
Output Logic High	$V_{OH}$	$V_{DD}-1.085$		$V_{DD}-0.880$	V
Output Logic Low	$V_{OL}$	$V_{DD}-1.830$		$V_{DD}-1.555$	V
Output Rise and Fall Time <sup>3</sup>					
Rise Time	$t_R$			1.0	ns
Fall Time	$t_F$			1.0	ns
Load		50 ohms into $V_{DD}-1.3V$			
Duty Cycle <sup>4</sup>		45	50	55	%
Jitter, 156M250 <sup>5</sup>	$\phi_J$				
12 kHz - 20 MHz			47	100	fs
12 kHz - 40 MHz			75	150	fs
10 kHz - 1 MHz			20	40	fs
1 kHz - 1 MHz			90	180	fs
1.875 MHz-20 MHz			45	90	fs
Period Jitter <sup>6</sup>	$\phi_J$				
RMS			1.3		ps
P/P			12		ps
Deterministic Jitter <sup>7</sup>			0		ps
Start-Up Time	$t_{SU}$			10	ms
Operating Temperature (Ordering Option)	$T_{OP}$	-10/70 or -40/85			°C
Package Size		5.0 x 7.0 x 1.8			mm

1. The VC-708 power supply pin should be filtered, e.g., a 10, 0.1, 0.01 and 0.001uf capacitors.
2. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
3. Figure 1 defines these parameters.
4. Duty Cycle is defined as the On Time/Period, see Figure 1.
5. Measured using an Agilent E5052.
6. Measured using a LeCroy Wavemaster 8600A, 90K samples, no filtering applied.
7. Measured using a Wavecrest SIA3300C, 90K samples.



**Figure 1.**

## Performance Specifications

**Table 2. Electrical Performance, LVDS**

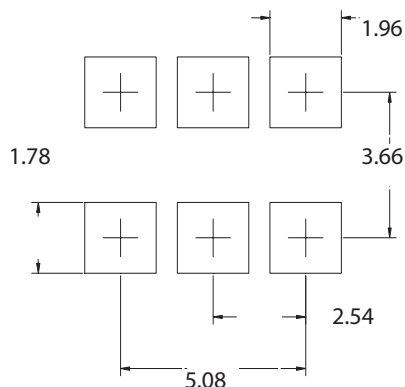
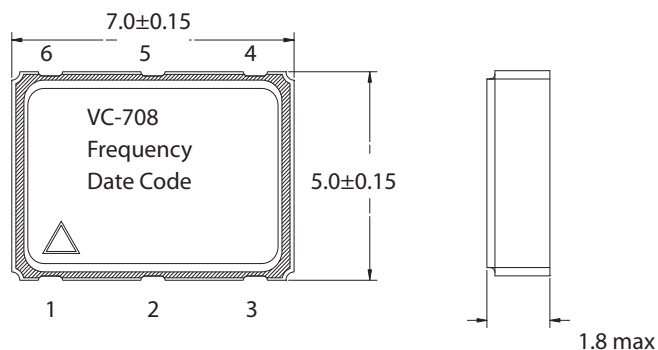
Parameter	Symbol	Min	Typical	Maximum	Units
<b>Supply</b>					
Voltage <sup>1</sup> (Ordering Option)	$V_{DD}$	3.135 2.375	3.3 2.5	3.465 2.625	V V
Current (No Load)	$I_{DD}$		37	48	mA
<b>Frequency</b>					
Nominal Frequency	$f_N$	See Table 9.			MHz
Stability <sup>2</sup> (Ordering Option)		±25, ±50, ±100			ppm
<b>Outputs</b>					
Differential Output Amplitude		247		454	mV
Differential Output Error		-50		50	mV
Offset Voltage		1.125	1.250	1.375	V
Offset Voltage Error		-50		50	mV
Output Rise and Fall Time <sup>3</sup>					
Rise Time	$t_R$			1.0	ns
Fall Time	$t_F$			1.0	ns
Load		100 ohms differential			
Duty Cycle <sup>3,4</sup>		45	50	55	%
Jitter 156.250MHz <sup>5</sup>	$\phi_J$				
12 kHz - 20 MHz			65	130	fs
12 kHz - 40 MHz			90	180	fs
10 kHz - 1 MHz			35	70	fs
1 kHz - 1 MHz			90	180	fs
1.875 MHz-20 MHz			63	120	fs
Period Jitter <sup>6</sup>	$\phi_J$				
RMS			1.3		ps
P/P			12		ps
Deterministic Jitter <sup>7</sup>			0		ps
Start-Up Time	$t_{SU}$			10	ms
Operating Temperature (Ordering Option)	$T_{OP}$	-10/70 or -40/85			°C
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1. The VC-708 power supply pin should be filtered, eg, a 10, 0.1, 0.01, 0.001uf capacitors.
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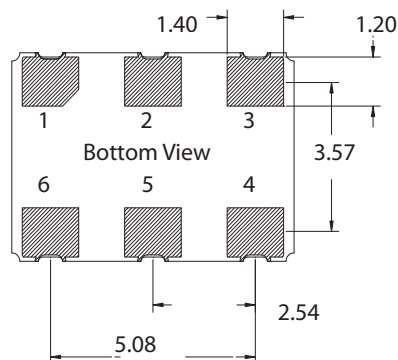
# Package and Pinout

**Table 3. Pinout**

Pin #	Symbol	Function
1	NC	No Internal Connection is made
2	NC	No Internal Connection is made
3	GND	Electrical and Lid Ground
4	$f_o$	Output Frequency
5	$Cf_o$	Complementary Output Frequency
6	$V_{DD}$	Supply Voltage



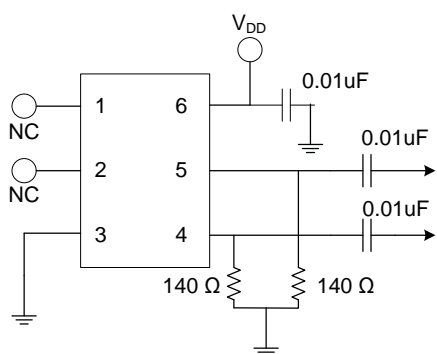
Units are mm



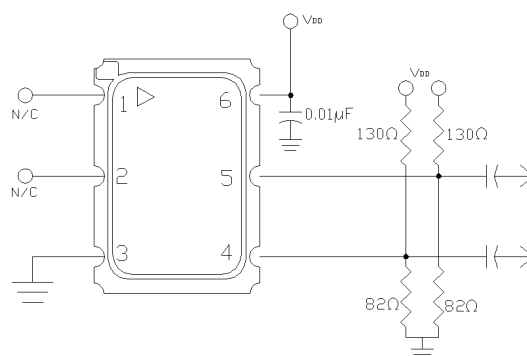
**Figure 2. Pad Layout**

**Figure 3. Package Outline Drawing**

# LVPECL Application Diagrams



**Figure 4. Single Resistor Termination Scheme**  
Resistor values are typically 140 ohms for 3.3V operation and 84 ohms for 2.5V operation.

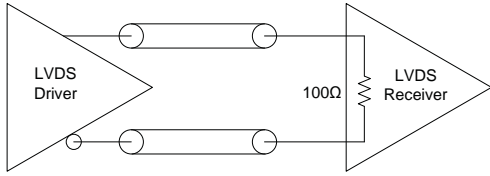


**Figure 5. Pull-Up Pull Down Termination**  
Resistor values shown are typical for 3.3 V operation. For 2.5V operation, the resistor to ground is 62 ohms and the resistor to supply is 250 ohms

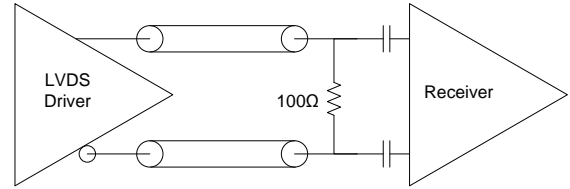
The VC-708 incorporates a standard PECL output scheme, which are unterminated FET drains. There are numerous application notes on terminating and interfacing PECL logic and the two most common methods are a single resistor to ground, Figure 4, and a pull-up/pull-down scheme as shown in Figure 5. AC coupling capacitor are optional, depending on the application and the input logic requirements of the next stage.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left unterminated, and if one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

## LVDS Application Diagrams



**Figure 6. LVDS to LVDS Connection, Internal 100ohm Resistor**  
Some LVDS structures have an internal 100 ohm resistor on the input and do not need additional components. AC blocking capacitors can be used if the DC levels are incompatible.



**Figure 7. LVDS to LVDS Connection**  
Some input structures may not have an internal 100 ohm resistor on the input and will need an external 100ohm resistor for impedance matching. Also, the input may have an internal DC bias which may not be compatible with LVDS levels, AC blocking capacitors can be used.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

## Environmental and IR Compliance

Table 4. Environmental Compliance	
Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002
Mechanical Vibration	MIL-STD-883 Method 2007
Temperature Cycle	MIL-STD-883 Method 1010
Solderability	MIL-STD-883 Method 2003
Fine and Gross Leak	MIL-STD-883 Method 1014
Resistance to Solvents	MIL-STD-883 Method 2015
Moisture Sensitivity Level	MSL1
Contact Pads	Gold over Nickel Gold thickness is 0.3-1.0um

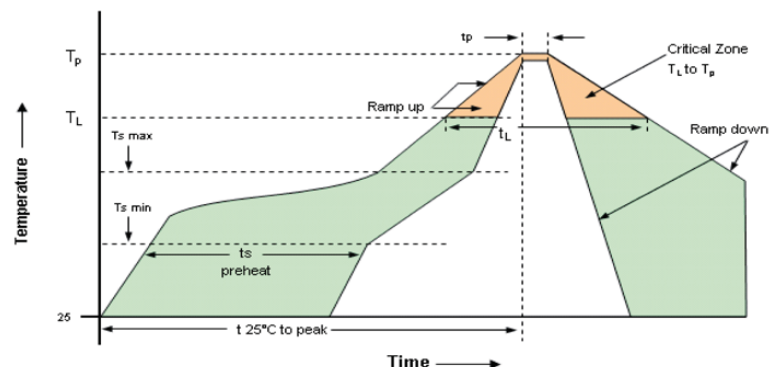
## IR Compliance

### Suggested IR Profile

Devices are built using lead free epoxy and can be subjected to standard lead free IR reflow conditions shown in Table 5. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220C.

Table 5. Reflow Profile		
Parameter	Symbol	Value
PreHeat Time	$t_s$	200 sec Max
Ramp Up	$R_{UP}$	3°C/sec Max
Time above 217°C	$t_L$	150 sec Max
Time to Peak Temperature	$t_{AMB-P}$	480 sec Max
Time at 260°C	$t_P$	30 sec Max
Time at 240°C	$t_{P2}$	60 sec Max
Ramp down	$R_{DN}$	6°C/sec Max

### Solderprofile:



## Maximum Ratings, Tape & Reel

### Absolute Maximum Ratings and Handling Precautions

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied or any other excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

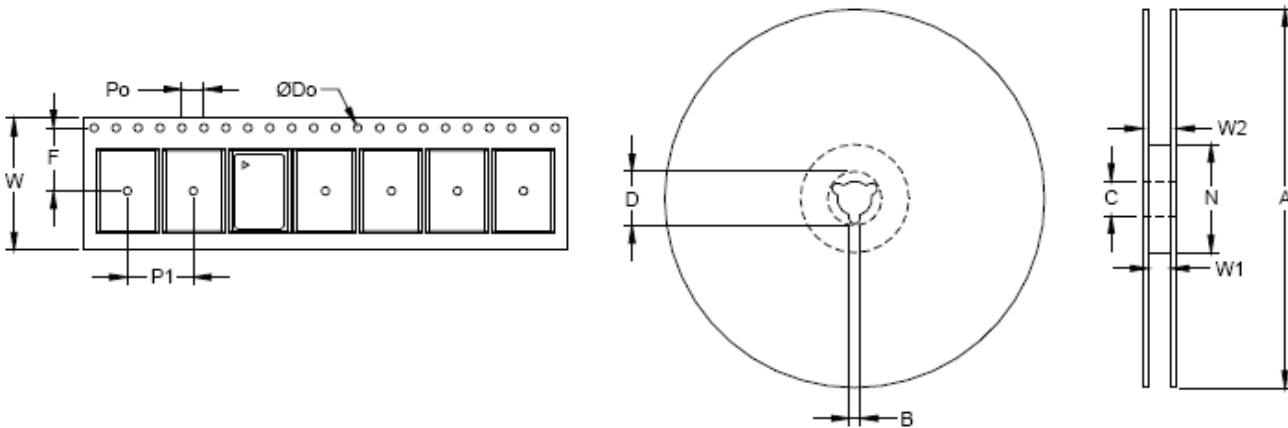
Although ESD protection circuitry has been designed into the VC-708, proper precautions should be taken when handling and mounting, VI employs a Human Body Model and Charged Device Model for ESD susceptibility testing and design evaluation.

ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM a standard resistance of 1.5kOhms and capacitance of 100pF is widely used and therefor can be used for comparison purposes.

Parameter	Symbol	Rating	Unit
Storage Temperature	$T_{STORE}$	-50/125	°C
Supply Voltage		-0.5 to 7.0	V
ESD, Human Body Model		1500	V
ESD, Charged Device Model		1000	V

**Table 7. Tape and Reel Information**

Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
16	7.5	1.5	4	8	180	2	13	21	55	17	21	250



## Ordering Information

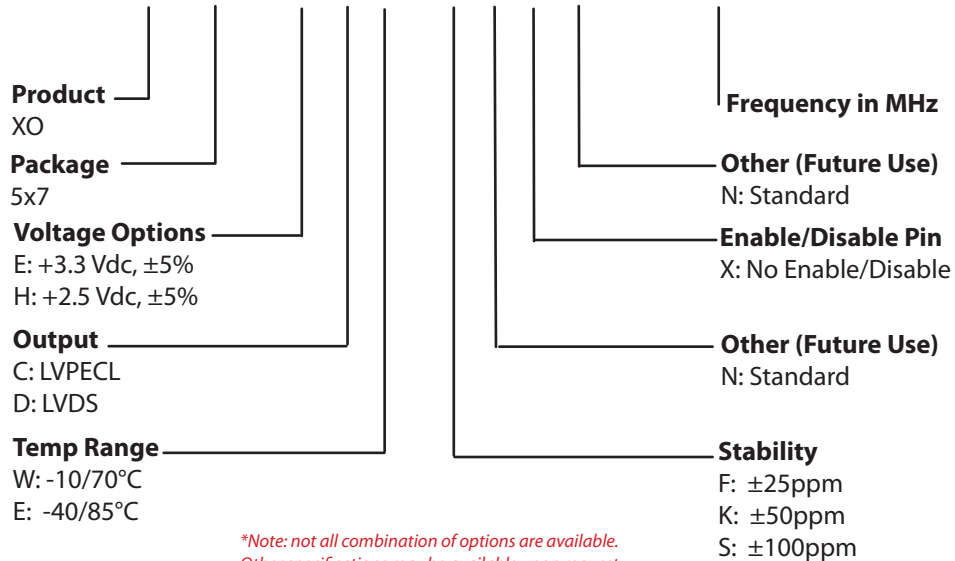
**Table 8. Standard Output Frequencies (MHz) LVPECL**

32.000	80.000	120.000	125.000	155.520	156.250	156.253906	156.257812
160.000	161.132800	161.132812	167.970	174.220	200.000		

**Table 9. Standard Output Frequencies (MHz) LVDS**

106M250	125M000	153M600	156M250	160M0000	161M1328	200M000	

### VC-708- E C E - K N X N - 156M250000



**Example: VC-708-ECE-KNXN-156M250000**

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